What is claimed is:

1. A semiconductor memory device having four pipelining latches for prefetching 4-bit data outputted from at least one bank in response to a start address of the 4-bit data and control signals, comprising:

a first data multiplexing means for receiving a first even datum from a first even line and a first odd datum from a first odd line and determining a data path of each of the first even and odd data between first & second data paths according to a data assigning control signal and outputting a first datum through the first data path and outputting a second datum through the second data path;

a second data multiplexing means for receiving a second even datum from a second even line and a second odd datum from a second odd line and determining a data path of each of the second even and odd data between third & forth data paths according to the data assigning control signal and outputting a third datum through the third data path and outputting a forth datum through the forth data path;

a third order multiplexing means for receiving the first datum from the first data path and the third datum from the third data path and sequentially outputting the first and the third data at a rising edge of a first control signal in response to the start address of the inputted data; and

a forth order multiplexing means for receiving the second datum from the second data path and the forth datum

from the forth data path and sequentially outputting the second and forth data to a falling edge of a second control signal in response to the start address of the inputted data,

wherein the 4-bit data is split into the first even data, the first odd data, the second even data and the second odd data, and the data assigning control signal is used for arranging a inputted data into a data path according to whether the start address of the inputted data is an even number or an odd number.

2. The semiconductor memory device of claim 1, wherein the first datum is the first even datum and the second datum is the first odd datum if the start address of the inputted 4-bit data is an even number, and the first datum is the first odd datum and the second datum is the first even datum if the start address of the inputted 4-bit data is an odd number.

3. The semiconductor memory device of claim 2, wherein the third datum is the second even datum and the forth datum is the second odd datum if the start address of the inputted 4-bit data is an even number, and the third datum is the second add datum and the forth datum is the second even datum if the start address of the inputted 4-bit data is an odd number.

4. The semiconductor memory device of claim 3, wherein the first multiplexing means includes:

a first data input block for receiving the first even data through the first even line in response to a input control signal;

a second data input block for receiving the first odd data through the odd line in response to the input control signal;

a first latch block for temporary storing the first even data outputted from the first data input block;

a second latch block for temporary storing the first odd data outputted from the second data input block;

a decision logic for receiving the starting address of the first even/odd data and outputting the data assigning control signal according to whether the starting address of the inputted 4-bit data is an odd number or an even number;

a first data output block for outputting the first even data to the first data path in response to the data assigning control signal; and

a second data output block for outputting the first odd data of the second data path in response to the data assigning control signal.

5. The semiconductor memory device of claim 4, wherein the second multiplexing means includes elements which serve as the elements included in the first multiplexing means.

6. The semiconductor memory device of claim 5, wherein the third multiplexing means sequentially outputs each of the

first datum and the third datum at each of a rising edge and a next rising edge of the first control signal in response to a predetermined value of the start address.

7. The semiconductor memory device of claim 6, wherein the forth multiplexing means sequentially outputs each of the second datum and the forth datum at a falling edge and a next falling edge of the second control signal in response to the predetermined value of the start address.

8. The semiconductor memory device of claim 7, wherein the third multiplexing means includes:

a first data select block having a first and a second passgates for passing the first datum and the third datum according to a third logical signal, gates of a PMOS transistor in the first passgate and a NMOS transistor in the second passgate being coupled to the third logical signal and gates of a NMOS transistor in the first passgate and a PMOS transistor in the second passgate being coupled to the inversed third logical signal; and

a first output control block having a first and a second PMOS transistors and a first and a second NMOS transistor which are serially connected between a supply voltage and a ground voltage, gates of the first PMOS transistor and the second NMOS transistor being coupled to a output signal of the data select block and gate of the second PMOS transistor being coupled to a rising edge output signal and gate of the first

NMOS transistor being coupled to the inversed rising edge output signal,

wherein the third logical signal is used for arranging an odd number times data in response to the start address and the rising edge output signal is used for outputting the output signal of the first data select block at a rising edge of a first and a second clock pulse.

9. The semiconductor memory device of claim 8, wherein the forth multiplexing means includes:

a second data select block having a third and a forth passgates for passing the first data and the third data according to a forth logical signal, gates of a PMOS transistor in the third passgate and a NMOS transistor in the forth passgate being coupled to the third logical signal and gates of a NMOS transistor in the forth passgate and a PMOS transistor in the forth passgate being coupled to the inversed forth logical signal; and

a second output control block having a third and a forth PMOS transistors and a third and a forth NMOS transistor which are serially connected between a supply voltage and a ground voltage, gates of the third PMOS transistor and the forth NMOS transistor being coupled to a output signal of the data select block and gate of the forth PMOS transistor being coupled to a falling edge output signal and gate of the third NMOS transistor being coupled to the inversed falling edge output signal,

wherein the forth logical signal is used for arranging an even number times data in response to the start address and the falling edge output signal is used for outputting the output signal of the second data select block at a falling edge of the first and the second clock pulse.

10. A semiconductor memory device for prefetching 4-bit data from at least one bank in response to an instruction for reading data, comprising:

a first control signal generating means for generating a first and a second control signals generated by logically combining a data input control signal with a data output control signal;

a second control signal generating means for generating a third control signal and a forth control signal, the third control signal generated by logically combining a odd enable signal which is used for outputting an odd times data with a odd arranging signal which is used for arranging the odd times data in response to a start address of the 4-bit data, the forth controls signal generated by logically combining a even enable signal which is used for outputting an even times data with a even arranging signal which is used for arranging the even times data in response to a start address of the 4-bit data; and

a signal delivering means controlled by the first, the second and the third control signals for outputting the 4-bit data to a first and a second even data output lines and a

first and a second odd data output lines.

11. The semiconductor memory device of claim 10, wherein the first control signal generating means includes:

an inverter receiving the data input control signal;

a first NAND gate for receiving the data output signal and an output of the inverter and generating the first control signal; and

a second NAND gate for receiving the output of the inverter and an output of the first NAND gate and generating the second control signal.

12. The semiconductor memory device of claim 11, wherein the second control signal generating means includes:

an odd data control block for generating the third control signal by logically combining the odd enable signal with the odd arranging signal; and

an even data control block for generating the forth control signal by logically combining the even enable signal with the even arranging signal.

13. The semiconductor memory device of claim 12, wherein the odd data control block includes:

an inverter receiving the odd enable signal;

a first NAND gate for receiving the odd arranging signal and an output of the inverter and generating a prior third control signal; and

a second NAND gate for receiving the output of the inverter and an output of the first NAND gate and generating a later third control signal.

14. The semiconductor memory device of claim 13, wherein the even data control block includes:

an inverter receiving the even enable signal;

a first NAND gate for receiving the even arranging signal and an output of the inverter and generating prior the forth control signal; and

a second NAND gate for receiving the output of the inverter and an output of the first NAND gate and generating later the forth control signal.

15. The semiconductor memory device of claim 14, wherein the signal delivering means includes:

a first data arranging unit controlled by the first control signal for arranging the inputted data;

a latch unit for temporary storing data outputted from the first data arranging unit; and

a second data arranging unit for arranging and outputting the stored data in the latch unit.

16. The semiconductor memory device of claim 15, wherein the first data arranging unit includes:

a first passgate for outputting a first data by the first control signal;

a second passgate for outputting a second data by the second control signal;

a third passgate for outputting a third data by the first control signal; and

a forth passgate for outputting a forth data by the second control signal.

17. The semiconductor memory device of claim 16, wherein the latch unit includes two inverters connected to each other for forming a loop with can latch a data.

18. The semiconductor memory device of claim 17, wherein the second data arranging unit outputs an inputted data in response to the prior or later third control signals.